International Research Journal on Advanced Engineering and Management
https://goldncloudpublications.com
https://doi.org/10.47392/IRJAEM.2025.0515

e ISSN: 2584-2854
Volume: 03 Issue: 12
December 2025
Page No: 3252 - 3262

Modeling and Analysis of Multilevel Inverter Topologies with Sustainable Energy

Anusha Rathi[1]*, Dr. C.S. Rajeshwari*[2]*, Dr. Anjali Potnis*[3]*, Dr. Anurag S.D. Rai*[4]
[1]*PhD Scholar, Dept. of EE, LNCT University, Bhopal, Madhya Pradesh, India.*
[2]*Professor, Dept. of EEE, NITTTR, Bhopal, Madhya Pradesh, India.*
[3]*Assistant Professor, Dept. of EEE, NITTTR, Bhopal, Madhya Pradesh, India.*
[4]*Professor, Dept. of EE, LNCT University, Bhopal, Madhya Pradesh, India.*
Emails: *anusha.anusha28@gmail.com*[1]*, csrajeshwari@nitttebpl.ac.in*[2]*, apotnis@nitttrbpl.ac.in*[3]*, anuragrai@lnct.ac.in*[4]

Abstract

Multilevel inverters (MLIs) have emerged as a foundational component in modern power electronics, particularly in medium- and high-voltage applications where conventional two-level inverters are no longer sufficient to meet performance, efficiency, and reliability standards. One of the primary motivations behind the widespread adoption of MLIs is their ability to synthesize high-quality output voltages with lower total harmonic distortion (THD), thereby improving power quality and system compatibility. This harmonic reduction is crucial in industrial and utility-scale applications, where precise voltage waveforms are essential for the reliable operation of motors, transformers, and sensitive loads. This paper introduces a novel multilevel inverter topology based on the cascaded connection of fundamental inverter modules. The proposed configuration is designed to operate efficiently in both symmetrical and asymmetrical modes, making it highly suitable for integration with renewable energy sources such as fuel cells and photovoltaic systems. In the symmetrical arrangement, each module utilizes identical DC source magnitudes, whereas in the asymmetrical configuration, unequal DC voltage levels—derived through binary or trinary progression—are employed to generate a greater number of output voltage levels using fewer components. The comparative analysis demonstrates that the proposed topology significantly reduces the number of power switches and passive components required, leading to lower power losses and enhanced overall inverter efficiency. Additionally, the total standing voltage stress on the semiconductor switches remains within acceptable limits, thereby improving reliability and operational safety compared to conventional multilevel inverter designs. The flexibility and simplicity of the proposed structure make it an ideal candidate for low- to medium-power renewable energy applications. To validate the functionality and effectiveness of the design, both simulation and experimental results are presented for 11-level, 15-level, and 19-level inverter configurations. The results confirm that the proposed inverter achieves high-quality output voltage waveforms with minimized harmonic distortion and improved performance across various load conditions.

Keywords: *Multilevel Converters, Modulation Techniques, Power Electronics.*

1. Introduction

In recent years, multilevel inverters (MLIs) have gained significant attention in medium-voltage industrial applications due to their superior performance over traditional two-level inverters. Two-level inverter configurations are generally unsuitable for medium-voltage applications because of the limited voltage-blocking capabilities of power semiconductor devices. MLIs, on the other hand, have emerged as an optimal solution for interfacing with medium-voltage grids, as they not only reduce the voltage stress (dv/dt) across semiconductor switches but also significantly lower total harmonic distortion (THD), thereby ensuring compliance with grid codes [1-3]. Furthermore, MLIs offer reduced power losses across switching devices and exhibit lower electromagnetic interference (EMI), enhancing their operational efficiency. Conventionally, multilevel inverter topologies are categorized into three main types: Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB). Among these, the CHB topology is widely preferred due to its modular nature, which facilitates scalability and adaptability for generating higher voltage levels. Despite these advantages, conventional MLI topologies face challenges as the number of output voltage levels increases. Specifically, the increase in levels leads to a proportional rise in the number of semiconductor devices and gate drivers, which complicates the overall design and control circuitry. Additionally, the presence of numerous discrete components can negatively impact the system's reliability and increase manufacturing costs. To address these limitations, several novel MLI topologies have been introduced in recent literature [4-6]. These include the Hybrid Series and Parallel Sources (HSPS), Crisscross Cascaded MLI, Packed U-Cells, and Cascaded Bipolar Switched Cells, among others. These emerging configurations aim to optimize the utilization of components while achieving superior output waveform quality with reduced complexity. In parallel with advancements in topology, significant research efforts have focused on developing and refining modulation strategies to enhance the performance of MLIs. Modulation techniques are broadly categorized based on their switching frequency. High-frequency modulation techniques—such as traditional Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Modulation (SVM)—are commonly employed in low- to medium-voltage applications due to their effectiveness in minimizing harmonic distortion. However, their use in medium-voltage scenarios is limited by the increase in switching losses, which can degrade overall system efficiency. In industrial applications, phase-shifted carrier-based SPWM remains widely adopted due to its capability to produce low-distortion output voltage waveforms. Figure 1. Shows the classification of MLI [6-9]. Meanwhile, Space Vector Modulation is particularly effective for three-level topologies, offering efficient control and utilization of the DC link voltage. Additionally, low switching frequency techniques such as staircase modulation, Space Vector Control (SVC), and Selective Harmonic Elimination (SHE) are gaining increased popularity for their efficiency and suitability in high-voltage scenarios.

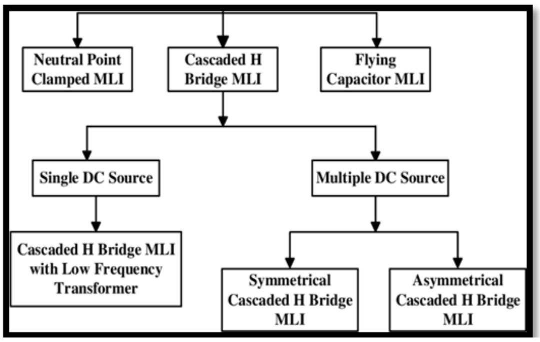

Figure 1 THE MLI Classification

1.1. Multilevel Inverter Topologies

The concept of multilevel inverters (MLIs) was first introduced in 1975, and since then, extensive research and development efforts have been dedicated to refining their structural design and operational performance. Over the years, various topologies have emerged, primarily focusing on modifications to the arrangement of semiconductor switches and the configuration of DC sources. One major direction of research has been aimed at achieving higher output power levels by utilizing power semiconductor switches in series along with multiple low-voltage DC sources [10-11]. This approach facilitates efficient power conversion and enables the synthesis of stepped voltage waveforms, often referred to as staircase waveforms. In practical implementations, DC voltage sources such as capacitors, batteries, or renewable energy systems (e.g., photovoltaic panels or wind turbines) are commonly used. These sources can be connected either individually or in combination, depending on the application and desired output characteristics. The general classification of multilevel inverter topologies is often based on their circuit structure and the manner in which voltage levels are generated. An overall classification scheme, typically illustrated in the literature, highlights the diversity of topologies based on their infrastructure. Although there are several methods to categorize MLIs, this paper adopts a classification based primarily on the nature of the DC source configuration. In this framework, MLIs are broadly divided into two categories: those utilizing a single DC source and those employing multiple DC sources. In the first category, a single DC source is used in conjunction with a carefully arranged network of capacitors and switches to generate multiple output voltage levels. This method relies on charging and discharging the capacitors in a controlled manner to achieve the required voltage steps [12]. The second category leverages multiple DC sources directly, allowing for greater flexibility in voltage level synthesis, particularly in modular and scalable inverter designs. This classification not only helps in understanding the structural differences between various MLI designs but also provides insight into their operational capabilities and suitability for different applications, especially in the context of integrating renewable energy systems. The Neutral Point Clamped (NPC) multilevel inverter topology is one of the most widely adopted configurations in industrial applications due to its structural simplicity, high efficiency, and capability to deliver substantial power levels. Introduced by Nabae et al. in 1981, the NPC inverter has become a benchmark solution, particularly for medium-voltage applications. Its defining feature is the inclusion of a neutral point that enables the generation of a zero-voltage level, thereby allowing the inverter to produce three distinct voltage levels: positive, zero, and negative. This feature contributes significantly to the reduction of output voltage harmonics. The topology operates by utilizing a series arrangement of capacitors to divide the total DC bus voltage into equal voltage segments [13]. This configuration, as depicted in typical NPC inverter circuit diagrams, facilitates voltage level synthesis without the need for multiple isolated DC sources. NPC inverters are especially effective under fundamental frequency switching conditions, making them suitable for medium-voltage grid-connected applications such as motor drives and reactive power compensation systems. However, one of the primary drawbacks of the NPC topology is its tendency to generate elevated levels of voltage and current total harmonic distortion (THD) under low switching frequencies. To counteract this, additional filtering components, such as reactors, are required, which can lead to increased system cost and complexity. Furthermore, as the number of voltage levels increases, the number of clamping diodes and capacitors must also be increased proportionally [14]. This not only escalates the component count and control complexity but also reduces the overall reliability of the system. Despite these limitations, the NPC inverter remains advantageous due to its inherent ability to reduce harmonic content by introducing intermediate voltage levels through neutral point clamping. While theoretically higher voltage levels can be achieved by adding more switching devices, diodes, and capacitors, practical implementations are typically limited to three levels. This limitation is primarily due to the challenge of maintaining voltage balance across the capacitors, which becomes increasingly difficult with more levels. Consequently, most real-world applications of NPC inverters are confined to three-level configurations. NPC inverters are commonly used in a wide range of high-power applications, including Static VAR Compensators (SVC), variable-speed motor drives, and interconnections in high-voltage transmission systems. Their modular design, robust performance, and compatibility with medium-voltage systems make them a preferred choice in industrial and utility-scale energy conversion systems [15]. Another prominent multilevel inverter topology utilizing a single DC source is the Flying Capacitor Multilevel Inverter (FC-MLI), which was introduced by Meynard et al. in 1992. The structural configuration of the FC-MLI closely resembles that of the Neutral Point Clamped (NPC) inverter; however, it replaces the clamping diodes with multiple capacitors to generate the intermediate voltage levels, as illustrated in typical circuit diagrams. This topology supports bidirectional power flow, making it capable of controlling both active and reactive power effectively [16]. Despite its advantages, the practical scalability of the FC-MLI is limited due to complexities in managing the charging and discharging cycles of the flying capacitors as the number of voltage levels increases. Figure 2 shows the NPC-MLI Topology This limitation imposes significant challenges in

International Research Journal on Advanced Engineering and Management
https://goldncloudpublications.com
https://doi.org/10.47392/IRJAEM.2025.0515
e ISSN: 2584-2854
Volume: 03 Issue: 12
December 2025
Page No: 3252 - 3262

maintaining voltage balance across the capacitors, necessitating the use of sophisticated control algorithms to ensure operational stability. Furthermore, as the voltage level increases, the number of capacitors required also grows, which not only increases the cost and physical size of the inverter but also reduces its overall reliability and service life.

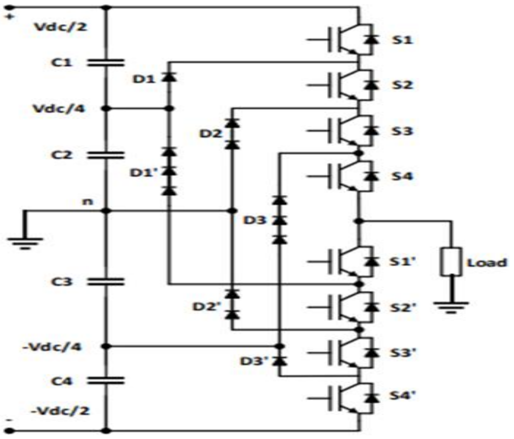

Figure 2 The NPC-MLI Topology

These challenges restrict the practical implementation of FC-MLIs to configurations with typically three to five voltage levels. Despite these drawbacks, FC-MLIs have found successful applications in several areas such as AC motor drives, active filters, Static VAR Compensators (SVC), and other switched converter systems, where their ability to manage reactive power and reduce harmonic content is especially beneficial. To overcome the limitations associated with single DC-source topologies, particularly in applications requiring higher voltage levels, multilevel inverter structures based on multiple DC sources have been developed. Among these, the Cascaded H-Bridge (CHB) topology is the most widely adopted [1-5]. The CHB configuration consists of several H-bridge cells connected in series on the AC side, with each cell powered by an independent DC source. These sources can be derived from batteries, fuel cells, or ultra-capacitors, offering a high degree of flexibility and scalability. One of the primary advantages of the CHB topology is its modular design, which simplifies control strategies and facilitates maintenance and fault management by isolating and bypassing individual cells when necessary. Unlike the NPC and FC-MLI configurations that typically rely on a single shared DC bus, each H-bridge cell in a CHB inverter operates with an isolated DC source. This isolation enhances system reliability and provides greater freedom in voltage level synthesis. Consequently, the CHB topology is well-suited for medium and high-power applications, particularly in renewable energy systems where multiple isolated DC sources are readily available. Its inherent modularity and scalability make the CHB inverter an attractive choice for modern power electronics systems that demand high efficiency, reliability, and reduced harmonic distortion [2-7]. The Cascaded H-Bridge Multilevel Inverter (CHB-MLI) is formed by connecting two or more single-phase H-bridge inverter units in series. This configuration derives its name from the original H-Bridge structure introduced in the late 1960s. By cascading multiple H-Bridge cells, the CHB-MLI produces a stepped voltage waveform composed of several discrete voltage levels. Each H-bridge unit contributes to the overall output by adding or subtracting its DC source voltage, enabling the synthesis of a multilevel output. Theoretically, by increasing the number of cascaded H-Bridge modules, the CHB-MLI can generate an unlimited number of voltage levels, offering a finely stepped approximation of a sinusoidal waveform. This makes it particularly advantageous for medium- and high-voltage applications where improved power quality and reduced harmonic distortion are critical [17].

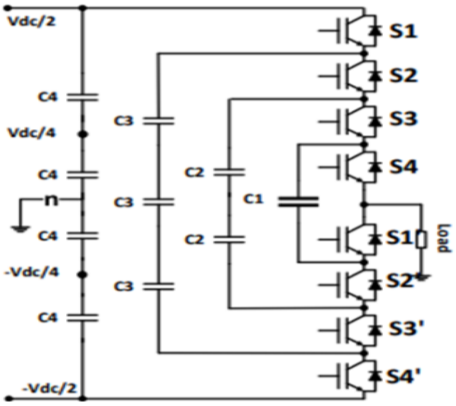

Figure 3 The FC-MLI Topology

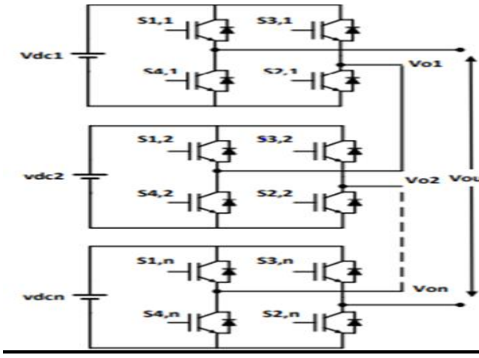

Figure 4 **Cascaded H-Bridge MLI Topology**

In the Cascaded H-Bridge Multilevel Inverter (CHB-MLI) topology, voltage and power levels can be easily scaled by increasing the number of H-bridge cells. However, this scalability comes with the significant requirement of several independent DC sources, which is one of the primary drawbacks of this configuration. Despite this, CHB-MLI offers the advantage of requiring fewer discrete components compared to other multilevel inverter topologies for a given number of output levels. Figure 3 shows the FC-MLI Topology and (b) Cascaded H-Bridge MLI Topology. The CHB-MLI is fundamentally composed of a series of H-bridge cells, each contributing to the synthesis of the desired stepped voltage waveform. This structure enables efficient control using various modulation techniques, such as Pulse Width Modulation (PWM), which enhances the precision and dynamic performance of the inverter. Due to its modularity and flexibility, the CHB-MLI is widely employed in diverse applications, including motor drives, electric vehicle propulsion systems, DC power source utilization, power factor correction, frequency link systems, and the integration of renewable energy sources. The subsequent section will explore the different advanced topologies derived from the basic CHB cell [18].

2. Topologies with H-Bridge

The Cascaded H-Bridge with Multiple Level DC Link (MLDCL) inverter was introduced by Gui Jia Su et al. [16] as a novel topology aimed at reducing switch count while maintaining high-quality multilevel output. An example of an MLDCL inverter with two input DC sources is depicted in Fig. 6. This configuration consists of 'n' cascaded half-bridge units, where each unit comprises a single DC source and two series-connected switches. These cascaded half-bridges form the "level-generation" stage, which produces a stepped DC voltage waveform. An H-Bridge is then employed to alternate the polarity of the output voltage, resulting in a full multilevel AC output waveform. Compared to traditional multilevel inverter (MLI) topologies, the MLDCL structure achieves the same number of output voltage levels with fewer semiconductor switches, thus enhancing efficiency and reducing implementation complexity [2]. A significant advantage of this topology is its compatibility with asymmetrical DC source configurations, offering greater flexibility in integrating varied energy sources. This topology is particularly well-suited for low-power applications (less than 100 kW), such as permanent magnet (PM) motor drives. The level-generation stage can utilize fast-switching semiconductors like Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), while the polarity-reversal H-Bridge can employ robust switches like Insulated-Gate Bipolar Transistors (IGBTs). Additionally, the MLDCL topology finds practical application in renewable energy systems, particularly in photovoltaic arrays and fuel cell-based power systems [17]. The following sections will explore more complex structures derived from this foundational cell design.

2.1. Switched Series/Parallel Sources (SSPS) based MLI topology

The Switched Series/Parallel Sources (SSPS)-based multilevel inverter (MLI) topology, introduced by Hinago et al. [18], is a notable advancement in MLI design.

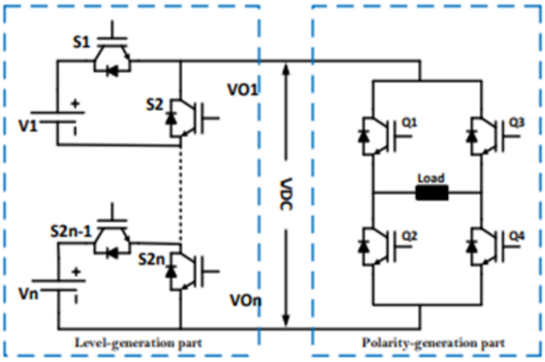

Figure 5 **The Circuit configuration of the MLDCL inverter**

This topology is composed of two main functional blocks: the level-generation part and the polarity-generation part. The level-generation section consists of multiple DC sources that produce a stepped DC voltage with a positive polarity. Figure 5 The Circuit configuration of the MLDCL inverter [19-23].

The polarity-generation section then converts this stepped DC voltage into an alternating current (AC) waveform, as illustrated in Fig. 6. One of the key advantages of this topology is its compatibility with asymmetric configurations, enabling it to generate a greater number of output voltage levels with fewer switching devices when compared to conventional MLI topologies [25-29]. This reduction in the number of switches not only simplifies the circuit but also improves efficiency and reduces the overall system cost. The SSPS-based MLI is especially attractive for electric vehicle (EV) applications, where the DC power source typically comprises several series-connected battery cells. These cells can be dynamically reconfigured using the SSPS topology to meet varying traction requirements. This re-configurability allows for greater flexibility in managing energy sources and optimizing power delivery, making the SSPS-based inverter a highly suitable choice for modern, energy-efficient EV powertrains and other mobile energy applications [17].

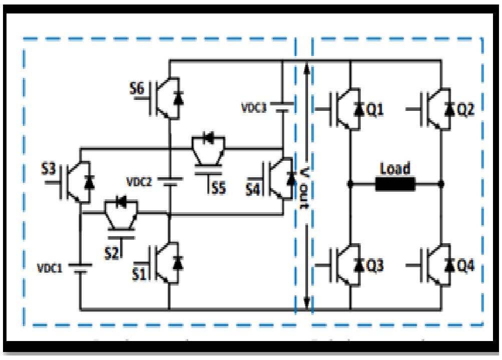

Figure 6 Circuit Configuration of the SSPS Inverter with Three DC Sources with Level-Generation Part Polarity-Generation Part

2.2. T-Type inverter topology

The T-Type inverter topology, introduced by Gerardo Ceglia et al. [19–21], represents a significant innovation in multilevel inverter design. Specifically developed as a five-level single-phase inverter, this configuration focuses on minimizing the number of semiconductor devices used. As shown in Fig. 7, the single-phase T-Type inverter employs twin voltage sources and a simplified structure that provides considerable improvements in terms of reduced switch count and streamlined circuit layout when compared to conventional multilevel inverter (MLI) topologies that achieve the same number of voltage levels. Figure 7. Shows the Circuit configuration for 5-level of the T-type inverter. One of the major advantages of the T-Type topology is its ability to reduce the number of primary power switches by approximately 40%, without the need for additional components like clamping diodes or balancing capacitors. The topology integrates a standard H-bridge along with an auxiliary bidirectional switch. This switch plays a critical role in controlling the connection of the DC voltage sources in such a way that a staircase-like AC output voltage waveform is constructed. However, a notable limitation of the T-Type inverter is its incompatibility with asymmetric source configurations. Due to the specific structure and limited switching states, it cannot accommodate varying DC input levels, thereby restricting its use to symmetrical configurations only [19]. Despite this limitation, the T-Type inverter offers a highly efficient and compact solution for applications requiring moderate voltage levels with a reduced component count and simplified control [30].

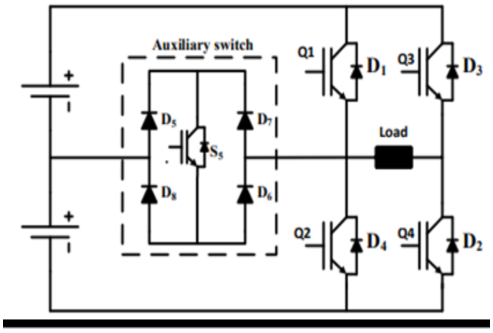

Figure 7 The Circuit configuration for 5-level of the T-type inverter

2.3. Crisscross Cascaded Multilevel Inverter (CCMLI) topology

The Crisscross Cascaded Multilevel Inverter

(CCMLI) topology is a recent advancement in the field of multilevel inverter designs aimed at achieving higher output voltage levels with fewer power electronic components. This topology modifies the traditional cascaded H-bridge structure by introducing a crisscross connection pattern between inverter cells and the associated DC sources. The unique interconnection of switches and sources allows for a more efficient utilization of the input DC voltages, enabling the generation of a greater number of output voltage levels with a reduced number of switches and isolated DC supplies. One of the key advantages of the Crisscross Cascaded MLI is its ability to produce a higher resolution output waveform, which leads to lower total harmonic distortion (THD), improved power quality, and reduced filter requirements [23]. Additionally, the crisscross arrangement provides better voltage balancing and switching redundancy, enhancing the overall fault tolerance and operational flexibility of the inverter. This makes it particularly suitable for renewable energy applications where multiple unequal or fluctuating DC sources, such as solar panels or battery units, are used. The CCMLI also supports modular expansion, allowing system designers to scale voltage levels as needed without significantly increasing system complexity or cost. Overall, the Crisscross Cascaded MLI topology represents a promising solution for efficient, compact, and high-performance power conversion in medium- to high-voltage energy systems.

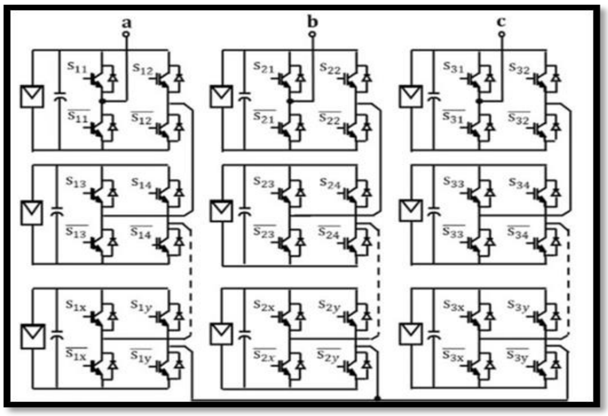

Figure 8 The Circuit Configuration for Multiple-Level with Two Dc Sources Cascaded Multilevel (CCMLI) Topology

2.3.1. Modulation Techniques

Various Classification of modulation techniques are shown in the Figure 7. Modulation strategies play a critical role in the operation of multilevel inverters, as they are responsible for generating the reference control signals and ensuring balanced voltage levels across all power sources. An effective multilevel modulation algorithm must meet several essential requirements to ensure optimal performance. These include delivering high-quality voltage output, maintaining a modular design, avoiding simultaneous switching of multiple voltage levels, minimizing the switching frequency of power devices to reduce switching losses, ensuring equal load sharing among all power modules, simplifying the control algorithm, and keeping implementation costs low [30, 21]. Among the key parameters influencing modulation performance, the modulation index stands out as particularly important. Depending on the modulation ratio, the system may operate in an over-modulation or under-modulation region, directly impacting the total harmonic distortion (THD) of the output waveform.

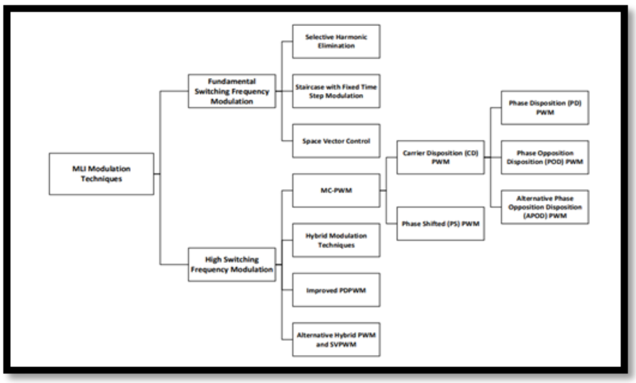

Figure 9 Various Classification of Modulation Techniques

To control multilevel inverters effectively, various modulation techniques have been developed, which can be broadly classified based on their switching frequency. These classifications include Fundamental Switching Frequency Modulation (FSFM) and High Switching Frequency Modulation (HSFM). FSFM operates at the fundamental frequency and typically produces lower switching losses, making it suitable for high-power applications. On the other hand, HSFM uses higher switching frequencies to achieve better waveform quality and lower THD, albeit at the cost of increased switching losses and thermal stress on power devices. The choice of modulation strategy depends on the specific application requirements, such as efficiency, harmonic performance, and system complexity [30]. Figure 8 shows the various classification of modulation techniques In both cases—whether fundamental or high switching frequency modulation is used—the output waveform of the multilevel inverter is obtained in a stepped or staired form. However, when high switching frequency methods are employed, these steps are further modulated using pulse width modulation (PWM) techniques. This additional modulation enhances the waveform quality by reducing total harmonic distortion (THD) and improving voltage regulation. The choice of modulation strategy directly influences the inverter's performance, including efficiency, harmonic content, and control complexity. To provide a clearer understanding of the available options, the various control techniques used for multilevel inverters have been systematically classified and are illustrated in Figure 8. This classification helps in selecting the appropriate modulation method based on application requirements such as power level, voltage quality, and system cost.

Fundamental Switching Frequency Modulation (FSFM) techniques operate at low switching frequencies, resulting in reduced switching losses and simplified control. These methods generate a staircase output waveform with one or two commutations per cycle. Notable FSFM techniques include Selective Harmonic Elimination PWM (SHE-PWM), which calculates optimal switching angles offline to eliminate specific low-order harmonics and minimize THD; Staircase with Fixed Time Step Modulation, which divides the waveform into equal time intervals for simplicity but introduces low-order harmonics; and Space Vector Control (SVC), which relies on space vector theory and does not synthesize a target voltage vector, distinguishing it from conventional SVM. These FSFM methods are advantageous for high-power applications due to their low switching loss and modular design scalability [3].

High Switching Frequency Modulation (HSFM) techniques enhance inverter performance by improving waveform quality through advanced PWM strategies. Among these, Multi-Carrier PWM (MC-PWM) uses multiple triangular carriers with a single sinusoidal modulating signal. It includes Carrier Disposition (CD) methods—Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposition Disposition (APOD)—which differ in the arrangement of carrier waveforms and influence harmonic distribution. Another approach is Phase-Shifted PWM (PS-PWM), where (n–1) triangular carriers are equally phase-shifted to achieve uniform switching and voltage balancing. Additionally, Hybrid PWM (H-PWM) combines low and high-frequency modulation to reduce switching losses, particularly in cascaded H-bridge inverters with unequal DC sources, thereby improving efficiency while maintaining output quality [30].

The Improved Phase Disposition PWM (PDPWM) technique, combined with Higher and Lower Carrier Cells and Alternative Phase Opposition (HLCCAPO), enhances traditional PDPWM by introducing two separate carrier groups—each with its own triangular waveform per carrier period. This modification effectively reduces switching losses, enabling operation at higher modulation frequencies. Additionally, it shifts energy from low-order to high-order harmonics, decreasing energy dissipation, and proving particularly effective for hybrid-clamped multilevel inverters (MLIs)[23-26]. In parallel, significant advancements have been made in Space Vector Pulse Width Modulation (SVPWM) for multilevel inverters. Amit Kumar Gupta and others developed a generalized SVPWM algorithm derived from standard two-level SVPWM. Their method simplifies the mapping process for multilevel inverter operation, even in the over-modulation range. Ahmed M. Massoud introduced both phase-shifted and hybrid SVM strategies for PWM generation in MLIs. Óscar López proposed a novel SVPWM algorithm for multilevel and multiphase voltage source converters, featuring switching state redundancy and FPGA-based implementation. Anish Gopinath explored the fractal structure of multilevel inverter space vector locations, which streamlined the SVPWM generation process by eliminating the need for lookup tables in sector identification [21]. Aneesh Mohamed A. S. introduced a technique for transforming standard two-level vectors into multilevel inverter output vectors by adding the center of a sub-hexagon, further simplifying the modulation process. Moreover, Mohan M. Renge presented a 3-D SVPWM technique to minimize common-mode voltage (CMV) at the output of multilevel inverters. SVPWM techniques offer several advantages over traditional sinusoidal PWM (SPWM), including better harmonic elimination and a fundamental voltage gain up to 15% higher than triangular carrier-based techniques. However, SVPWM requires complex sector identification and switching interval calculations, especially as the number of levels increases [29]. Despite this complexity, the implementation of SVPWM is feasible with the aid of digital signal processors (DSPs) and microprocessors. For three-phase n-level inverters, the SVPWM space vector diagram consists of six sectors, each containing $(n-1)^2$ vector combinations and n^3 possible switching states, making SVPWM a powerful but intricate control method for multilevel inverter applications.

Conclusion

Multilevel inverters (MLIs) have emerged as the most efficient solution for DC to AC power conversion in medium and high voltage applications. This paper provides a comprehensive review of both conventional and recently developed MLI topologies. It discusses the fundamental building blocks of MLIs and their wide-ranging applications. Recent innovations have focused on reducing the number of components, significantly impacting the overall size, cost, reliability, and efficiency of inverter systems. Notably, the development of topologies that support asymmetric DC sources has expanded the applicability of MLIs in higher voltage domains. These features make MLIs particularly well-suited for grid-connected systems, especially in renewable energy applications such as photovoltaic and wind energy integration. Furthermore, a variety of modulation strategies are explored, each offering specific benefits that enhance inverter performance and reduce total harmonic distortion (THD). The diversity of modulation techniques contributes to better control and efficiency, further strengthening the suitability of MLIs in modern power systems. Ongoing research into MLI topologies, control strategies, and applications continues to evolve in response to the growing demand for renewable energy integration and smart grid technologies.

Acknowledgements

I would like to express my sincere gratitude to my guide, Dr. Anurag S. D. Rai, for their continuous support, valuable guidance, and encouragement throughout this research work. I am also thankful to the faculty members of Department Electrical Engineering for their insightful comments and suggestions. This research would not have been possible without the guidance and support of Dr. Jitendra Tandekar and Dr. Sudhir Sharma My sincere thanks to my peers and colleagues for their constructive discussions and assistance. Lastly, I am deeply indebted to my family for their unwavering encouragement.

References

[1]. F. Khoucha, M. S. Lagoun, A. Kheloui, and M. E. H. Benbouzid, “A Comparison of Symmetrical and Asymmetrical Three-Phase H-Bridge Multilevel Inverter for DTC Induction Motor Drives,” IEEE Transactions on Energy Conversion, vol. 26, no. 1, pp. 64-72, 2011.
[2]. L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel inverters for electric vehicle applications." pp. 79-84.
[3]. A. Bendre, S. Krstic, J. V. Meer, and G. Venkataramanan, “Comparative evaluation of modulation algorithms for neutral-point-clamped converters,” IEEE Transactions on Industry Applications, vol. 41, no. 2, pp. 634-643, 2005.
[4]. A. Nabae, I. Takahashi, and H. Akagi, “A New Neutral-Point-Clamped PWM Inverter,” IEEE Transactions on Industry Applications, vol. IA-17, no. 5, pp. 518-523, 1981.
[5]. G. Joos, H. Xiaogang, and O. Boon Teck, "Direct-coupled multilevel cascaded series

VAr compensators." pp. 1608-1615 vol.2.

[6]. L. A. Tolbert, P. Fang Zheng, T. Cunnyngham, and J. N. Chiasson, “Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles,” IEEE Transactions on Industrial Electronics, vol. 49, no. 5, pp. 1058-1064, 2002.

[7]. Siddique, M.D.; Mekhilef, S.; Shah, N.M.; Memon, M.A. Optimal Design of a New Cascaded Multilevel Inverter Topology With Reduced Switch Count. IEEE Access 2019, 7, 24498–24510.

[8]. Koohi-Fayegh, S.; Rosen, M.A. A review of energy storage types, applications and recent developments. J. Energy Storage 2020, 27, 101047.

[9]. Vijeh, M.; Rezanejad, M.; Samadaei, E.; Bertilsson, K. A general review of multilevel inverters based on main submodules: Structural point of view. IEEE Trans. Power Electron. 2019, 34, 9479–9502.

[10]. Bana, P.R.; Panda, K.P.; Naayagi, R.; Siano, P.; Panda, G. Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: Topologies, comprehensive analysis and comparative evaluation. IEEE Access 2019, 7, 54888–54909.

[11]. Kumari, M.; Siddique, M.D.; Sarwar, A.; Tariq, M.; Mekhilef, S.; Iqbal, A. Recent trends and review on switched-capacitor-based single stage boost multilevel inverter. Int. Trans. Elect. Energy Syst. 2021, 31, e12730.

[12]. Khan, M.N.H.; Forouzesh, M.; Siwakoti, Y.P.; Li, L.; Blaabjerg, F. Switched capacitor integrated (2n+1)-level step-up single-phase inverter. IEEE Trans. Power Electron. 2020, 35, 8248–8260.

[13]. Nakagawa, Y.; Koizumi, H. A boost-type nine-level switched capacitor inverter. IEEE Trans. Power Electron. 2019, 34, 6522–6532.

[14]. Barzegarkhoo, R.; Siwakoti, Y.P.; Aguilera, R.P.; Khan, M.N.H.; Lee, S.S.; Blaabjerg, F. A novel dual-mode switched-capacitor five-level inverter with common-ground transformerless concept. IEEE Trans. Power Electron. 2021, 36, 13740–13753.

[15]. Khan, M.N.H.; Siwakoti, Y.P.; Scott, M.J.; Li, L.; Khan, S.A.; Lu, D.D.C.; Barzegarkhoo, R.; Sidorski, F.; Blaabjerg, F.; Hasan, S.U. A common grounded type dual-mode five-level transformerless inverter for photovoltaic applications. IEEE Trans. Ind. Electron. 2021, 68, 9742–9754.

[16]. Ye, Y.; Chen, S.; Zhang, X.; Yi, Y. Half-bridge modular switched capacitor multilevel inverter with hybrid pulsewidth modulation. IEEE Trans. Power Electron. 2020, 35, 8237–8247.

[17]. Saeedian, M.; Adabi, M.E.; Hosseini, S.M.; Adabi, J.; Pouresmaeil, E. A novel step-up single source multilevel inverter: Topology, operating principle, and modulation. IEEE Trans. Power Electron. 2019, 34, 3269–3282.

[18]. Saeedian, M.; Adabi, M.E.; Adabi, J. Step-up switched-capacitor module for cascaded MLI topologies. IET Power Electron. 2018, 11, 1286–1296.

[19]. Jahan, H.K. A new transformerless inverter with leakage current limiting and voltage boosting capabilities for grid-connected PV applications. IEEE Trans. Ind. Electron. 2020, 67, 10542–10551.

[20]. Ye, Y.; Chen, S.; Hua, T.; Lin, M.; Wang, X. Self-balanced multilevel inverter with hybrid double- and half-mode switched capacitor. IEEE Trans. Ind. Electron. 2022, 69, 5735–5744.

[21]. Sarwer, Z.; Siddique, M.D.; Sarwar, A.; Zaid, M.; Iqbal, A.; Mekhilef, S. A switched-capacitor multilevel inverter topology employing a novel variable structure nearest-level modulation. Int. Trans. Elect. Energy Syst. 2021, 31, e13151.

[22]. Anand, V.; Singh, V. A 13-level switched-capacitor multilevel inverter with single dc source. IEEE J. Emerg. Sel. Topics Power Electron. 2022, 10, 1575–1586. [.] 38. Roy, T.; Tesfay, M.W.; Nayak, B.; Panigrahi, C.K. A 7-level switched capacitor multilevel

inverter with reduced switches and voltage stresses. IEEE Trans. Circuits Syst. II Exp. Briefs 2021, 68, 3587–3591

[23]. Sharma, P.; Naidu, R.C. Optimization techniques for grid-connected PV with retired EV batteries in centralized charging station with challenges and future possibilities: A review. Ain Shams Eng. J. 2023, 14, 101985.

[24]. Barzegarkhoo, R.; Zamiri, E.; Moradzadeh, M.; Shadabi, H. Symmetric hybridised design for a novel step-up 19-level inverter. IET Power Electron. 2017, 10, 1377–1391.

[25]. Taheri, A.; Rasulkhani, A.; Ren, H. A multilevel inverter using switched-capacitors with reduced components. IET Power Electron. 2020, 13, 3954–3962.

[26]. Rawa, M. Dual input switched-capacitor-based single-phase hybrid boost multilevel inverter topology with reduced number of component. IET Power Electron. 2020, 13, 881–891.

[27]. Iqbal, A.; Siddique, M.D.; Reddy, B.P.; Maroti, P.K.; Alammari, R. A new family of step-up hybrid switched-capacitor integrated multilevel inverter topologies with dual input voltage sources. IEEE Access 2021, 9, 4398–4410.

[28]. Raman, S.R.; Fong, Y.C.; Ye, Y.; Cheng, K.W.E. Family of multiport switched-capacitor multilevel inverters for high-frequency ac power distribution. IEEE Trans. Power Electron. 2019, 34, 4407–4422.

[29]. Raman, S.R.; Cheng, K.W.E.; Ye, Y. Multi-input switched capacitor multilevel inverter for high-frequency AC power distribution. IEEE Trans. Power Electron. 2018, 33, 5937–5948.

[30]. Arif, M.; Siddique, M.; Ahmad, S.; Iqbal, A.; Ashique, R.; Ayob, S. An improved asymmetrical multilevel inverter topology with boosted output voltage and reduced component count. IET Power Electron. 2021, 12, 2052–2066.